

KM681000B Family

CMOS SRAM

128K x8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.6 $\mu$ m CMOS
- Organization : 128Kx8
- Power Supply Voltage : Single 5.0V  $\pm$ 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard  
32-DIP, 32-SOP, 32-TSOP I R/F

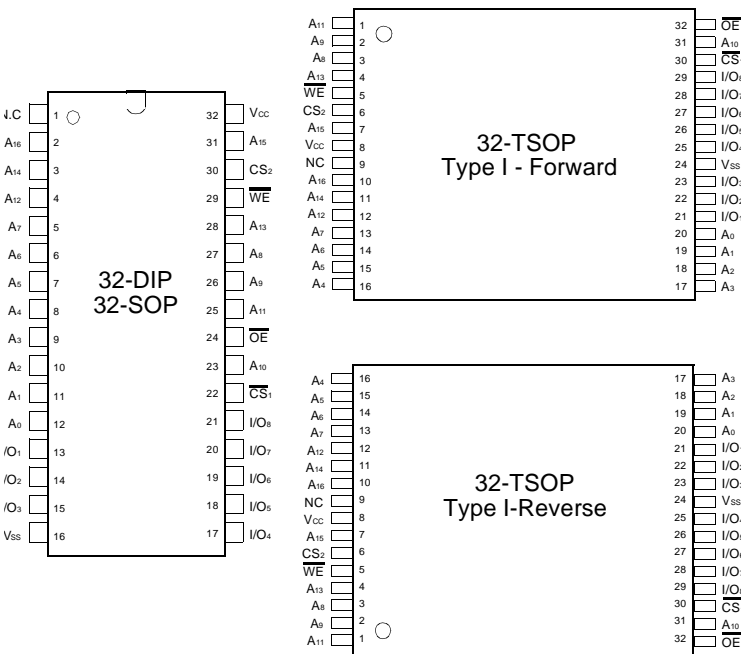
GENERAL DESCRIPTION

The KM681000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

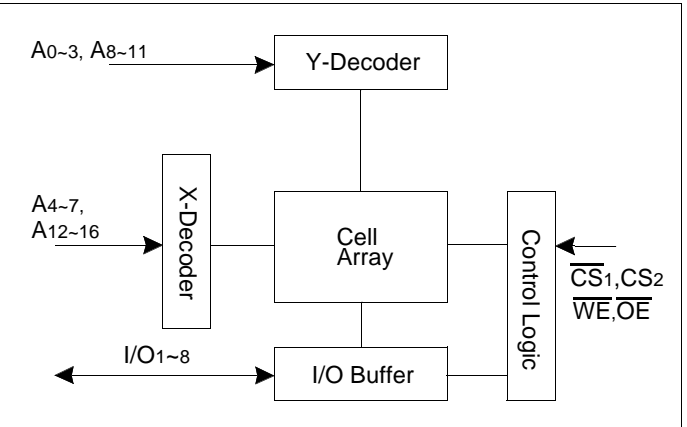
PRODUCT FAMILY

| Product Family               | Operating Temperature        | Speed    | PKG Type                       | Power Dissipation                |                               |
|------------------------------|------------------------------|----------|--------------------------------|----------------------------------|-------------------------------|
|                              |                              |          |                                | Standby (I <sub>SB1</sub> , Max) | Operating (I <sub>CC2</sub> ) |
| KM681000BL<br>KM681000BL-L   | Commercial(0~7 $\circ$ C)    | 55/70ns  | 32-DIP,32-SOP<br>32-TSOP I R/F | 100 $\mu$ W<br>20 $\mu$ W        | 70mA                          |
| KM681000BLE<br>KM681000BLE-L | Extended(-25~85 $\circ$ C)   | 70/100ns | 32-SOP<br>32-TSOP I R/F        | 100 $\mu$ W<br>50 $\mu$ W        |                               |
| KM681000BLI<br>KM681000BLI-L | Industrial(-40~85 $\circ$ C) | 70/100ns | 32-SOP<br>32-TSOP I R/F        | 100 $\mu$ W<br>50 $\mu$ W        |                               |

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



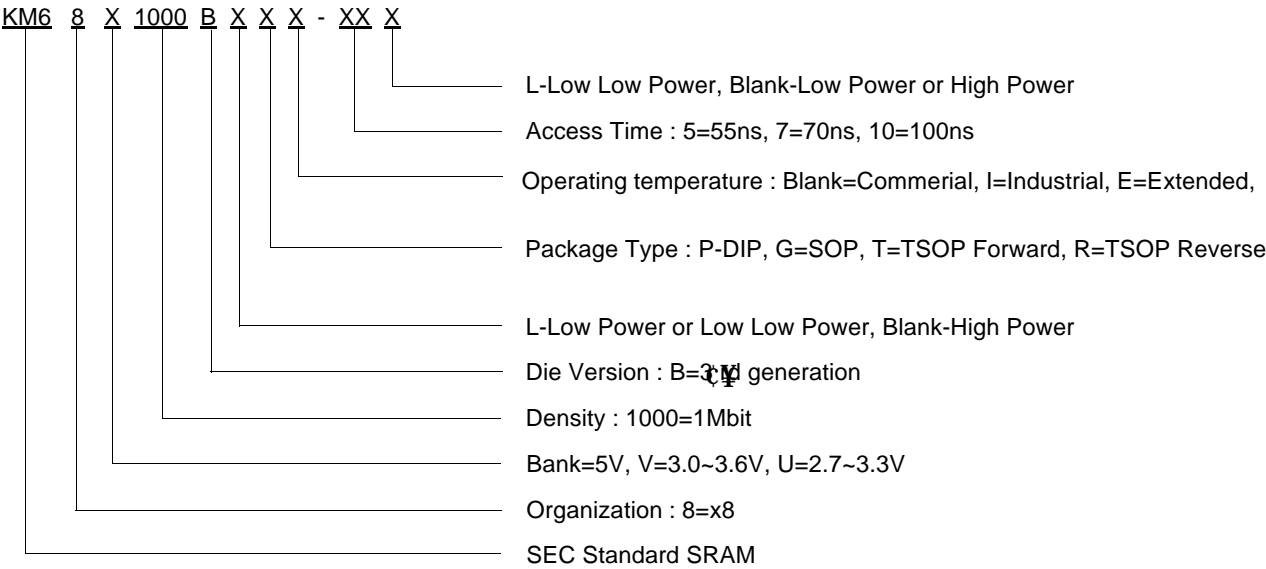
| Name                                  | Function            |
|---------------------------------------|---------------------|
| A <sub>0</sub> ~A <sub>16</sub>       | Address Inputs      |
| $\overline{WE}$                       | Write Enable Input  |
| $\overline{CS_1}$ , $\overline{CS_2}$ | Chip Select Inputs  |
| $\overline{OE}$                       | Output Enable Input |
| I/O <sub>1</sub> ~I/O <sub>18</sub>   | Data Inputs/Outputs |
| V <sub>CC</sub>                       | Power               |
| V <sub>SS</sub>                       | Ground              |
| N.C                                   | No Connection       |

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

| Commercial Temp Product<br>(0~70;E) |                       | Extended Temp Products<br>(-25~85;E) |                        | Industrial Temp Products<br>(-40~85;E) |                        |
|-------------------------------------|-----------------------|--------------------------------------|------------------------|--|------------------------|
| Part Name                           | Function              | Part Name                            | Function               | Part Name                              | Function               |
| KM681000BLP-5                       | 32-DIP,55ns,L-pwr     | KM681000BLGE-7                       | 32-SOP,70ns,L-pwr      | KM681000BLGI-7                         | 32-SOP,70ns,L-pwr      |
| KM681000BLP-5L                      | 32-DIP,55ns,LL-pwr    | KM681000BLGE-7L                      | 32-SOP,70ns,LL-pwr     | KM681000BLGI-7L                        | 32-SOP,70ns,LL-pwr     |
| KM681000BLP-7                       | 32-DIP,70ns,L-pwr     | KM681000BLGE-10                      | 32-SOP,100ns,L-pwr     | KM681000BLGI-10                        | 32-SOP,100ns,L-pwr     |
| KM681000BLP-7L                      | 32-DIP,70ns,LL-pwr    | KM681000BLGE-10L                     | 32-SOP,100ns,LL-pwr    | KM681000BLGI-10L                       | 32-SOP,100ns,LL-pwr    |
| KM681000BLG-5                       | 32-SOP,55ns,L-pwr     | KM681000BLTE-7                       | 32-TSOP F,70ns,L-pwr   | KM681000BLTI-7                         | 32-TSOP F,70ns,L-pwr   |
| KM681000BLG-5L                      | 32-SOP,55ns,LL-pwr    | KM681000BLTE-7L                      | 32-TSOP F,70ns,LL-pwr  | KM681000BLTI-7L                        | 32-TSOP F,70ns,LL-pwr  |
| KM681000BLG-7                       | 32-SOP,70ns,L-pwr     | KM681000BLTE-10                      | 32-TSOP F,100ns,L-pwr  | KM681000BLTI-10                        | 32-TSOP F,100ns,L-pwr  |
| KM681000BLG-7L                      | 32-SOP,70ns,LL-pwr    | KM681000BLTE-10L                     | 32-TSOP F,100ns,LL-pwr | KM681000BLTI-10L                       | 32-TSOP F,100ns,LL-pwr |
| KM681000BLT-5                       | 32-TSOP F,55ns,L-pwr  | KM681000BLRE-7                       | 32-TSOP R,70ns,L-pwr   | KM681000BLRI-7                         | 32-TSOP R,70ns,L-pwr   |
| KM681000BLT-5L                      | 32-TSOP F,55ns,LL-pwr | KM681000BLRE-7L                      | 32-TSOP R,70ns,LL-pwr  | KM681000BLRI-7L                        | 32-TSOP R,70ns,LL-pwr  |
| KM681000BLT-7                       | 32-TSOP F,70ns,L-pwr  | KM681000BLRE-10                      | 32-TSOP R,100ns,L-pwr  | KM681000BLRI-10                        | 32-TSOP R,100ns,L-pwr  |
| KM681000BLT-7L                      | 32-TSOP F,70ns,LL-pwr | KM681000BLRE-10L                     | 32-TSOP R,100ns,LL-pwr | KM681000BLRI-10L                       | 32-TSOP R,100ns,LL-pwr |
| KM681000BLR-5                       | 32-TSOP R,55ns,L-pwr  |                                      |                        |  |                        |
| KM681000BLR-5L                      | 32-TSOP R,55ns,LL-pwr |                                      |                        |  |                        |
| KM681000BLR-7                       | 32-TSOP R,70ns,L-pwr  |                                      |                        |  |                        |
| KM681000BLR-7L                      | 32-TSOP R,70ns,LL-pwr |                                      |                        |  |                        |

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS\*

| Item                                  | Symbol   | Ratings                  | Unit | Remark           |
|---------------------------------------|----------|--------------------------|------|------------------|
| Voltage on any pin relative to Vss    | VIN,VOUT | -0.5 to 7.0              | V    | -                |
| Voltage on Vcc supply relative to Vss | VCC      | -0.5 to 7.0              | V    | -                |
| Power Dissipation                     | PD       | 1.0                      | W    | -                |
| Storage temperature                   | TSTG     | -65 to 150               | °C   | -                |
| Operating Temperature                 | TA       | 0 to 70                  | °C   | KM681000BL/L-L   |
|                                       |          | -25 to 85                | °C   | KM681000BLE/LE-L |
|                                       |          | -40 to 85                | °C   | KM681000BLI/LI-L |
| Soldering temperature and time        | TSOLDER  | 260°C, 10sec (Lead Only) | -    | -                |

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS\*

| Item               | Symbol | Min     | Typ** | Max     | Unit |
|--------------------|--------|---------|-------|---------|------|
| Supply voltage     | VCC    | 4.5     | 5.0   | 5.5     | V    |
| Ground             | VSS    | 0       | 0     | 0       | V    |
| Input high voltage | VIH    | 2.2     | -     | VCC+0.5 | V    |
| Input low voltage  | VIL    | -0.5*** | -     | 0.8     | V    |

1) Commercial Product : TA=0 to 70°C, unless otherwise specified  
2) Extended Product : TA=-25 to 85°C, unless otherwise specified  
3) Industrial Product : TA=-40 to 85°C, unless otherwise specified  
\*\* TA=25°C  
\*\*\* VIL(min)=-3.0V for tA 50ns pulse width

CAPACITANCE\* (f=1MHz, TA=25°C)

| Item                     | Symbol | Test Condition | Min | Max | Unit |
|--------------------------|--------|----------------|-----|-----|------|
| Input capacitance        | CIN    | Vin=0V         | -   | 6   | pF   |
| Input/Output capacitance | CIO    | Vio=0V         | -   | 8   | pF   |

\* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

| Item                           |               | Symbol           | Test Conditions*   |                    | Mi  | Typ** | Max   | Unit |
|--------------------------------|---------------|------------------|--|--------------------|-----|-------|-------|------|
| Input leakage current          |               | I <sub>LI</sub>  | V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>  |                    | -1  | -     | 1     | Œ    |
| Output leakage current         |               | I <sub>LO</sub>  | CS <sub>1</sub> =V <sub>IH</sub> or CS <sub>2</sub> =V <sub>IL</sub> or WE=V <sub>IL</sub> , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub> |                    | -1  | -     | 1     | Œ    |
| Operating power supply current |               | I <sub>CC</sub>  | CS <sub>1</sub> =V <sub>IL</sub> , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>IO</sub> =0mA |                    | -   | 7     | 15**  | mA   |
| Average operating current      |               | I <sub>CC1</sub> | Cycle time=1Œ 100% duty<br>CS <sub>1</sub> 0.2V, CS <sub>2</sub> V <sub>CC</sub> -0.2V   |                    | -   | -     | 10*** | mA   |
|                                |               | I <sub>CC2</sub> | I <sub>IO</sub> =0mA CS <sub>1</sub> =V <sub>IL</sub> ,CS <sub>2</sub> =V <sub>IH</sub><br>Min cycle, 100% duty                                  |                    | -   | -     | 70    | mA   |
| Output low voltage             |               | V <sub>OL</sub>  | I <sub>OL</sub> =2.1mA   |                    | -   | -     | 0.4   | V    |
| Output high voltage            |               | V <sub>OH</sub>  | I <sub>OH</sub> =-1.0mA  |                    | 2.4 | -     | -     | V    |
| Standby Current(TTL)           |               | I <sub>SB</sub>  | CS <sub>1</sub> =V <sub>IH</sub> , CS <sub>2</sub> =V <sub>IL</sub>  |                    | -   | -     | 3     | mA   |
| Standby Current (CMOS)         | KM681000BL    | I <sub>SB1</sub> | CS <sub>1</sub> V <sub>CC</sub> -0.2V<br>CS <sub>2</sub> V <sub>CC</sub> -0.2V or<br>CS <sub>2</sub> 0.2V<br>Other input=0~V <sub>CC</sub>       | L (Low Power)      | -   | -     | 100   | Œ    |
|                                | KM681000BL-L  |                  |  | LL (Low Low Power) | -   | -     | 20    | Œ    |
|                                | KM681000BLE   |                  |  | L (Low Power)      | -   | -     | 100   | Œ    |
|                                | KM681000BLE-L |                  |  | LL (Low Low Power) | -   | -     | 50    | Œ    |
|                                | KM681000BLI   |                  |  | L (Low Power)      | -   | -     | 100   | Œ    |
|                                | KM681000BLI-L |                  |  | LL (Low Low Power) | -   | -     | 50    | Œ    |

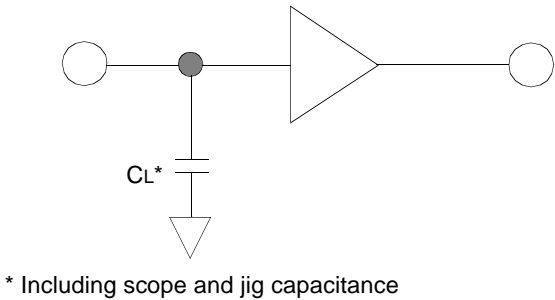
\* 1) Commercial Product : T<sub>A</sub>=0 to 70°C, V<sub>CC</sub>=5.0V ±10%, unless otherwise specified  
2) Extended Product : T<sub>A</sub>=-25 to 85°C, V<sub>CC</sub>=5.0V ±10%, unless otherwise specified  
2) Industrial Product : T<sub>A</sub>=-40 to 85°C, V<sub>CC</sub>=5.0V ±10%, unless otherwise specified  
\*\* 20mA for Extended and Industrial Products  
\*\*\* 15mA for Extended and Industrial Products

A.C CHARACTERISTICS

TEST CONDITIONS(1.Test Load and Test Input/Output Reference)\*

| Item                               | Value                      | Remark |
|------------------------------------|----------------------------|--------|
| Input pulse level                  | 0.8 to 2.4V                | -      |
| Input rising & falling time        | 5ns                        | -      |
| input and output reference voltage | 1.5V                       | -      |
| Output load (See right)            | C <sub>L</sub> =100pF+1TTL | -      |

\* See DC Operating conditions



TEST CONDITIONS(2. Temperature and Vcc Conditions)

| Product Family   | Temperature | Power Supply(Vcc) | Speed Bin | Comments   |
|------------------|-------------|-------------------|-----------|------------|
| KM681000BL/L-L   | 0~70jE      | 5.0Vj%10%         | 55/70ns   | Commercial |
| KM681000BLE/LE-L | -25~85jE    | 5.0Vj%10%         | 70/100ns  | Extended   |
| KM681000BLI/LI-L | -40~85jE    | 5.0Vj%10%         | 70/100ns  | Industrial |

PARAMETER LIST FOR EACH SPEED BIN

| Parameter List |                                 | Symbol    | Speed Bins |     |      |     |       |     | Units |
|----------------|---------------------------------|-----------|------------|-----|------|-----|-------|-----|-------|
|                |                                 |           | 55ns       |     | 70ns |     | 100ns |     |       |
|                |                                 |           | Min        | Max | Min  | Max | Min   | Max |       |
| Read           | Read cycle time                 | tRC       | 55         | -   | 70   | -   | 100   | -   | ns    |
|                | Address access time             | tAA       | -          | 55  | -    | 70  | -     | 100 | ns    |
|                | Chip select to output           | tCO1,tCO2 | -          | 55  | -    | 70  | -     | 100 | ns    |
|                | Output enable to valid output   | tOE       | -          | 25  | -    | 35  | -     | 50  | ns    |
|                | Chip select to low-Z output     | tLZ1,tLZ2 | 10         | -   | 10   | -   | 10    | -   | ns    |
|                | Output enable to low-Z output   | tOLZ      | 5          | -   | 5    | -   | 5     | -   | ns    |
|                | Chip disable to high-Z output   | tHZ1,tHZ2 | 0          | 20  | 0    | 25  | 0     | 30  | ns    |
|                | Output disable to high-Z output | tOHZ      | 0          | 20  | 0    | 25  | 0     | 30  | ns    |
|                | Output hold from address change | tOH       | 10         | -   | 10   | -   | 10    | -   | ns    |
| Write          | Write cycle time                | tWC       | 55         | -   | 70   | -   | 100   | -   | ns    |
|                | Chip select to end of write     | tCW       | 45         | -   | 60   | -   | 80    | -   | ns    |
|                | Address set-up time             | tAS       | 0          | -   | 0    | -   | 0     | -   | ns    |
|                | Address valid to end of write   | tAW       | 45         | -   | 60   | -   | 80    | -   | ns    |
|                | Write pulse width               | tWP       | 40         | -   | 50   | -   | 60    | -   | ns    |
|                | Write recovery time             | tWR       | 0          | -   | 0    | -   | 0     | -   | ns    |
|                | Write to output high-Z          | tWHZ      | 0          | 20  | 0    | 25  | 0     | 30  | ns    |
|                | Data to write time overlap      | tDW       | 25         | -   | 30   | -   | 40    | -   | ns    |
|                | Data hold from write time       | tDH       | 0          | -   | 0    | -   | 0     | -   | ns    |
|                | End write to output low-Z       | tOW       | 5          | -   | 5    | -   | 5     | -   | ns    |

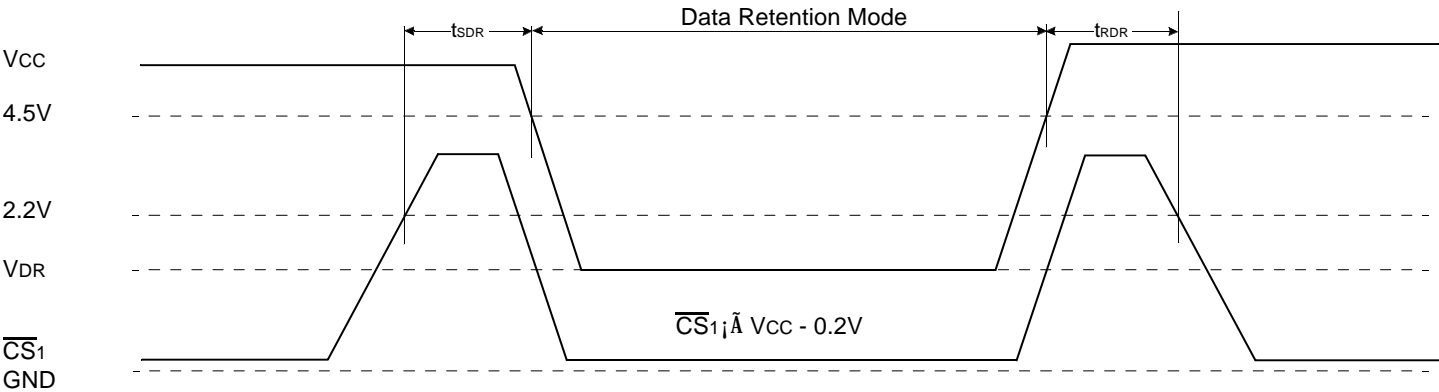
DATA RETENTION CHARACTERISTICS

| Item                       | Symbol |                              | Test Condition*  |                 | Min    | Typ**    | Max      | Unit    |
|----------------------------|--------|------------------------------|--|-----------------|--------|----------|----------|---------|
| Vcc for data retention     | VDR    |                              | $\overline{CS}_1^{***} \hat{A} V_{CC}-0.2V$            |                 | 2.0    | -        | 5.5      | V       |
| Data retention current     | IDR    | KM681000BL<br>KM681000BL-L   | $V_{CC}=3.0V$<br>$\overline{CS}_1 \hat{A} V_{CC}-0.2V$ | L-Ver<br>LL-Ver | -<br>- | 1<br>0.5 | 50<br>10 | $\mu A$ |
|                            |        | KM681000BLE<br>KM681000BLE-L |  | L-Ver<br>LL-Ver | -<br>- | -<br>-   | 50<br>25 |         |
|                            |        | KM681000BLI<br>KM681000BLI-L |  | L-Ver           | -      | -        | 50       |         |
|                            |        |                              |  | LL-Ver          | -      | -        | 25       |         |
| Data retention set-up time | tRDR   |                              | See data retention waveform                            |                 | 0      | -        | -        | ms      |
| Recovery time              | tRDR   |                              |  |                 | 5      | -        | -        |         |

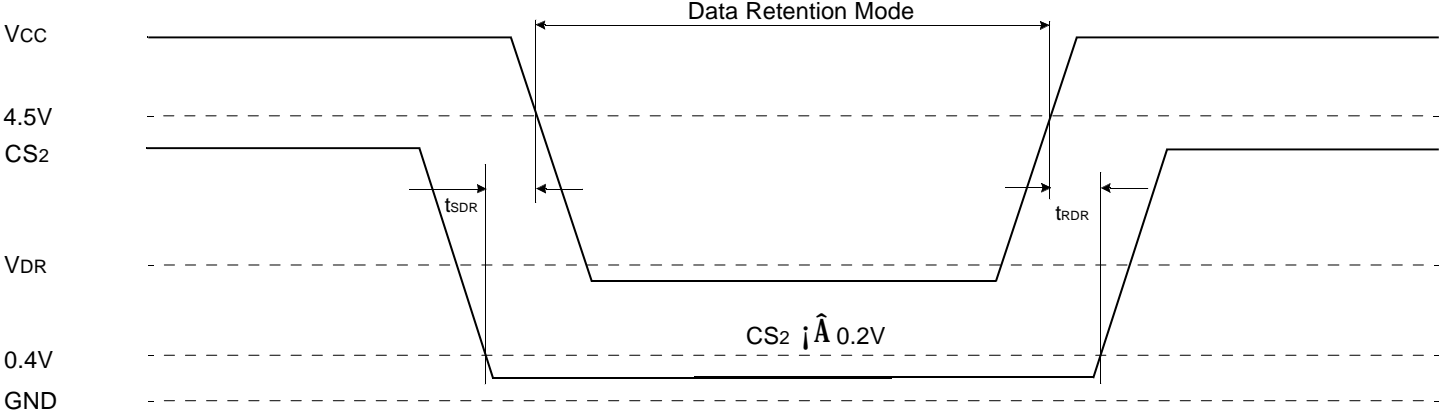
\* 1) Commercial Product : TA=0 to 70°C, unless otherwise specified  
2) Extended Product : TA=-25 to 85°C, unless otherwise specified  
2) Industrial Product : TA=-40 to 85°C, unless otherwise specified  
\*\* TA=25°C  
\*\*\*  $\overline{CS}_1 \hat{V}_{CC}-0.2V, CS_2 \hat{V}_{CC}-0.2V$ ( $\overline{CS}_1$  controlled) or  $CS_2 \hat{V}_{CC}-0.2V$ ( $CS_2$  controlled)

DATA RETENTION TIMING DIAGRAM

1)  $\overline{CS}_1$  Controlled

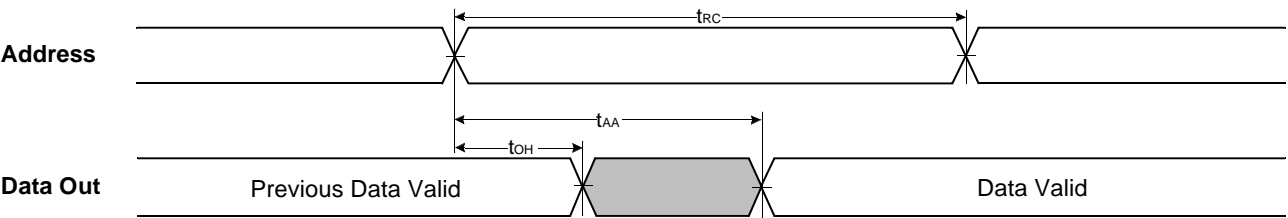


2)  $CS_2$  controlled

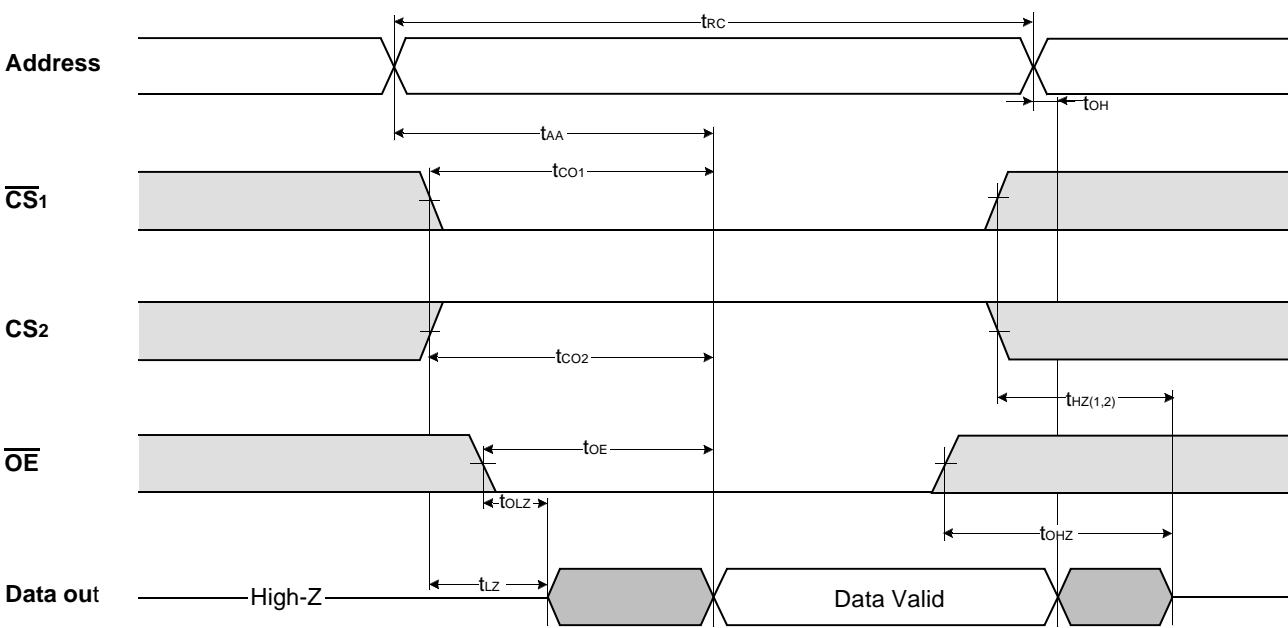


**TIMMING DIAGRAMS**

**TIMING WAVEFORM OF READ CYCLE (1)**  
 (Address Controlled)  
 ( $\overline{CS_1}=\overline{OE}=V_{IL}$ ,  $CS_2=\overline{WE}=V_{IH}$ )



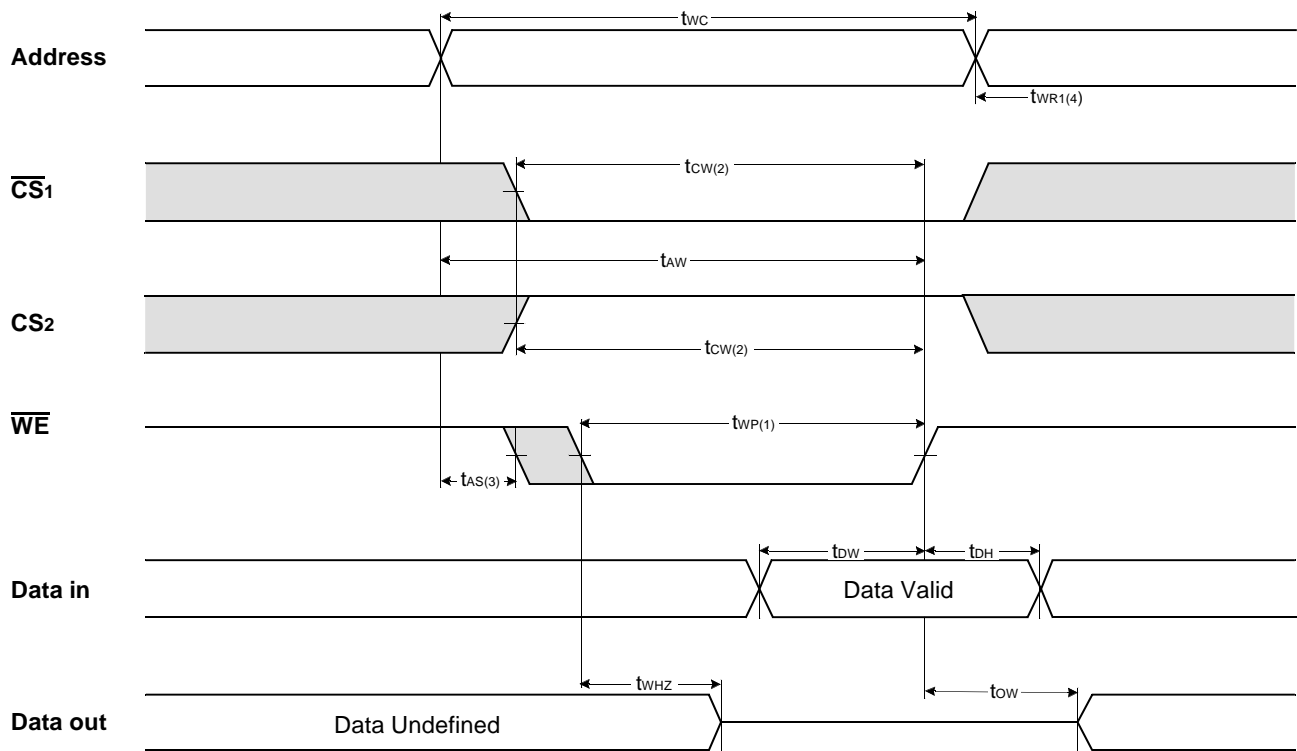
**TIMING WAVEFORM OF READ CYCLE (2)**  
 ( $\overline{WE}=V_{IH}$ )



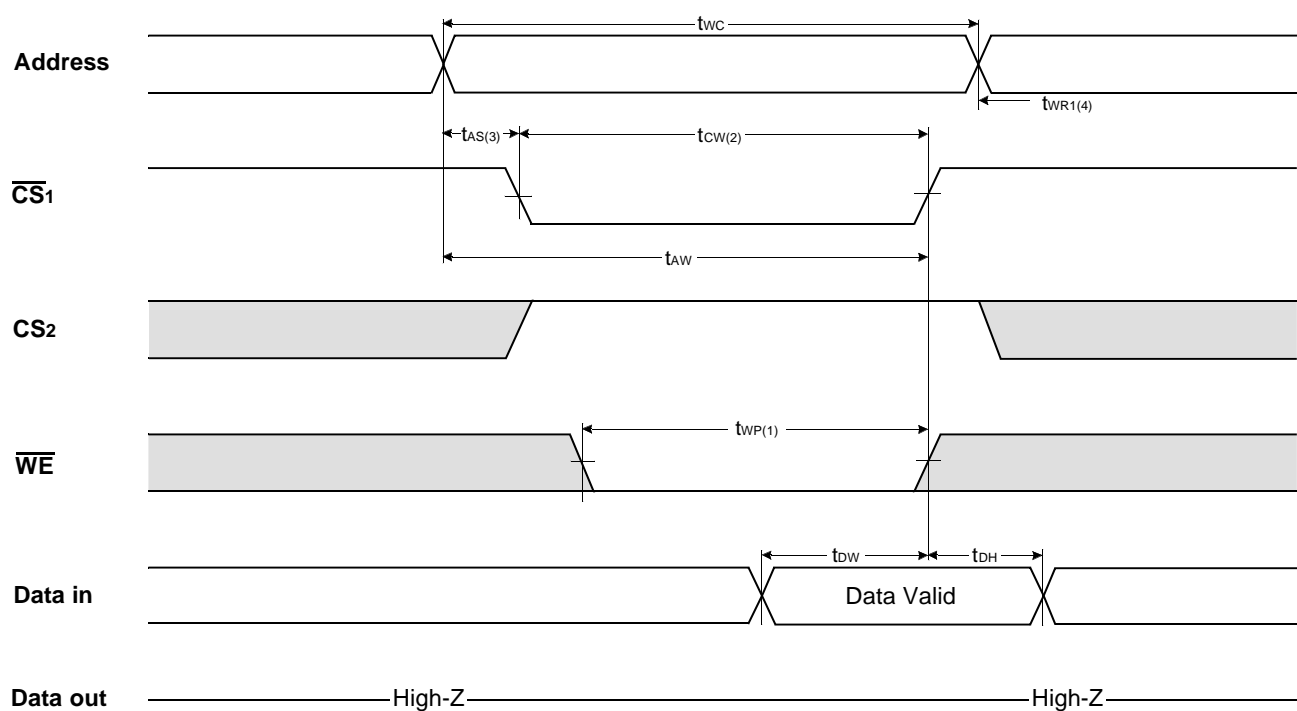
**NOTES (READ CYCLE)**

- 1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition,  $t_{HZ}(\text{max.})$  is less than  $t_{LZ}(\text{min.})$  both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (1)  $\overline{WE}$  Controlled

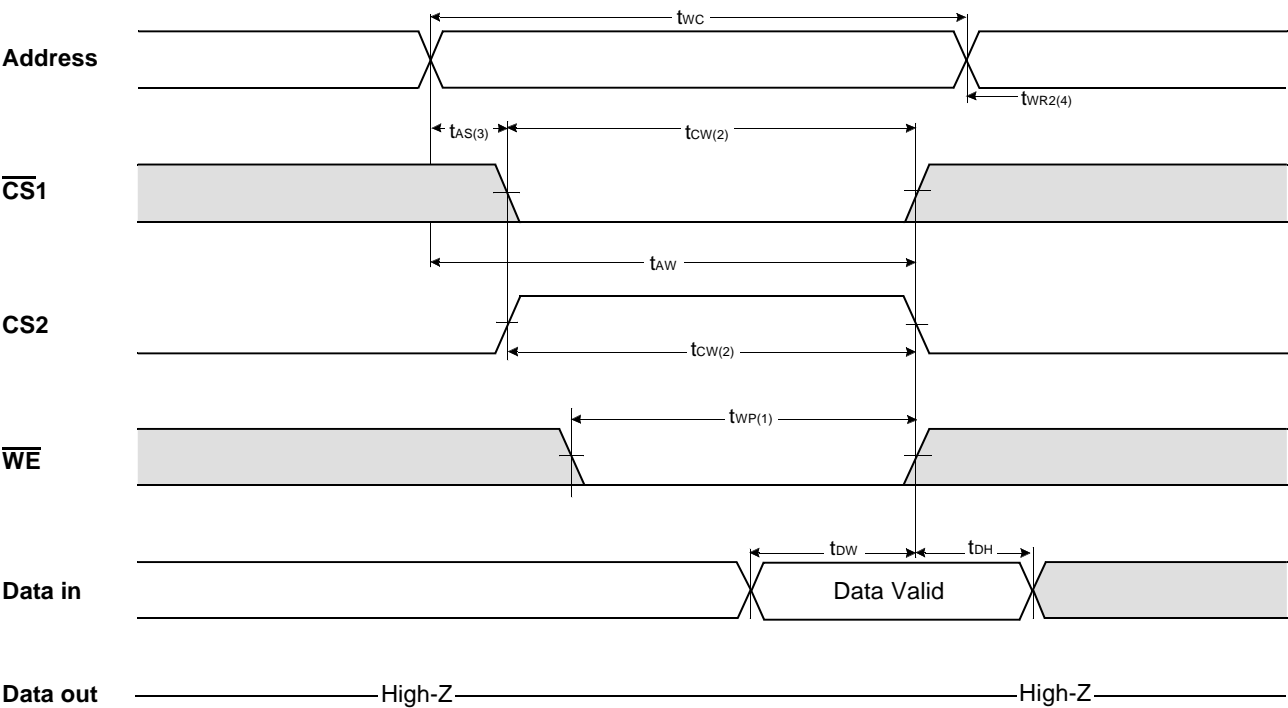


TIMING WAVEFORM OF WRITE CYCLE (2)  $\overline{CS_1}$  Controlled





TIMING WAVEFORM OF WRITE CYCLE (2 $\overline{CS_2}$  Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap of low  $\overline{CS_1}$ , high  $CS_2$  and low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS_1}$  going low,  $CS_2$  going high and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS_1}$  going high,  $CS_2$  going low and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning or write to the end of write.
- 2.  $t_{CW}$  is measured from the later of  $\overline{CS_1}$  going low or  $CS_2$  going high to the end of write.
- 3.  $t_{AS}$  is measured from the address valid to the beginning of write.
- 4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR1}$  applied in case a write ends at  $\overline{CS_1}$ , or  $\overline{WE}$  going high,  $t_{WR2}$  applied in case a write ends at  $CS_2$  going to low.

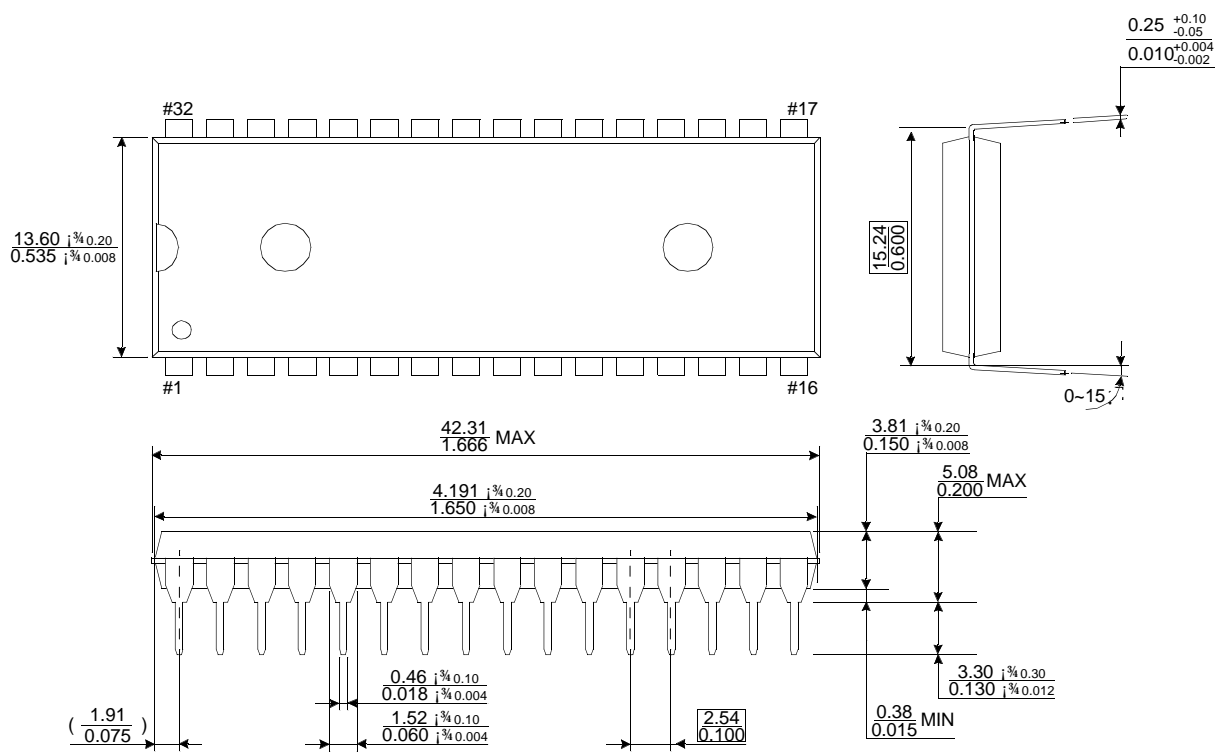
FUNCTIONAL DESCRIPTION

| $\overline{CS_1}$ | $CS_2$ | $\overline{WE}$ | $\overline{OE}$ | Mode           | I/O Pin | Current Mode      |
|-------------------|--------|-----------------|-----------------|----------------|---------|-------------------|
| H                 | X      | X               | X               | Power Down     | High-Z  | $I_{SB}, I_{SB1}$ |
| X                 | L      | X               | X               | Power Down     | High-Z  | $I_{SB}, I_{SB1}$ |
| L                 | H      | H               | H               | Output Disable | High-Z  | $I_{CC}$          |
| L                 | H      | H               | L               | Read           | Dout    | $I_{CC}$          |
| L                 | H      | L               | X               | Write          | Din     | $I_{CC}$          |

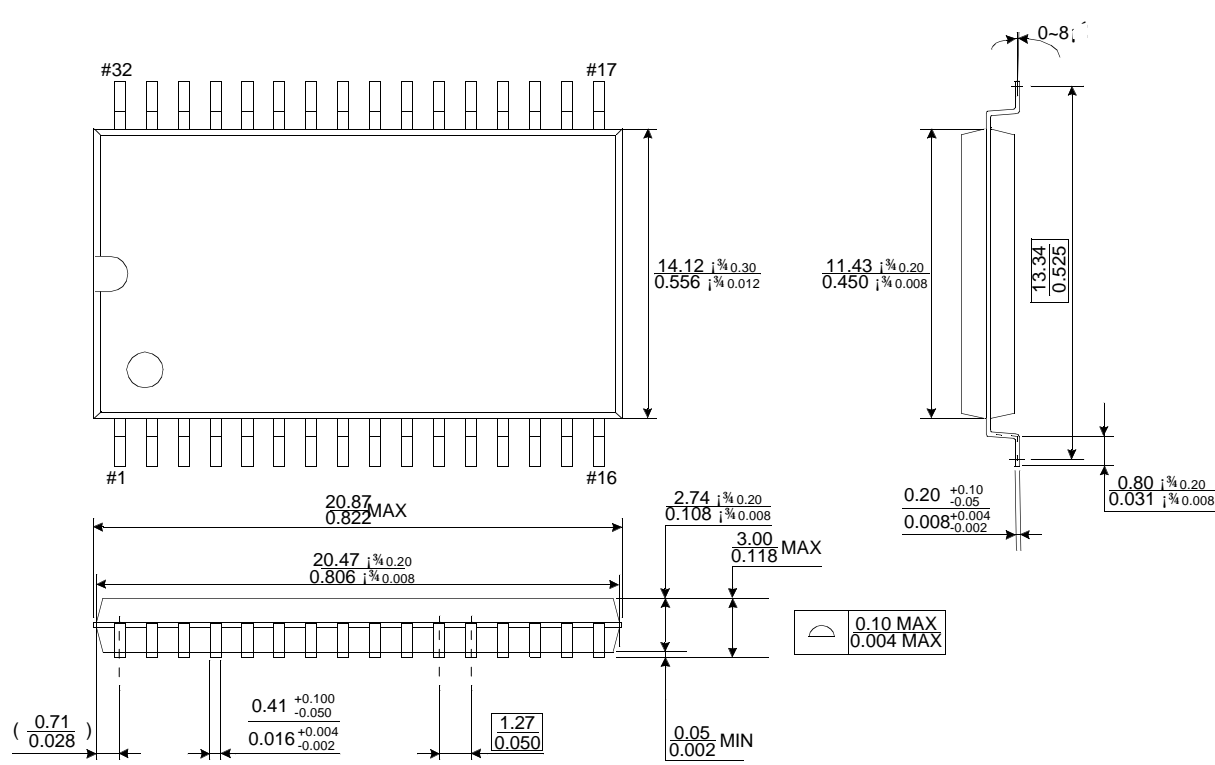
\* X means don't care

PACKAGE DIMENSIONS
 Units :MillimeterS(Inches)

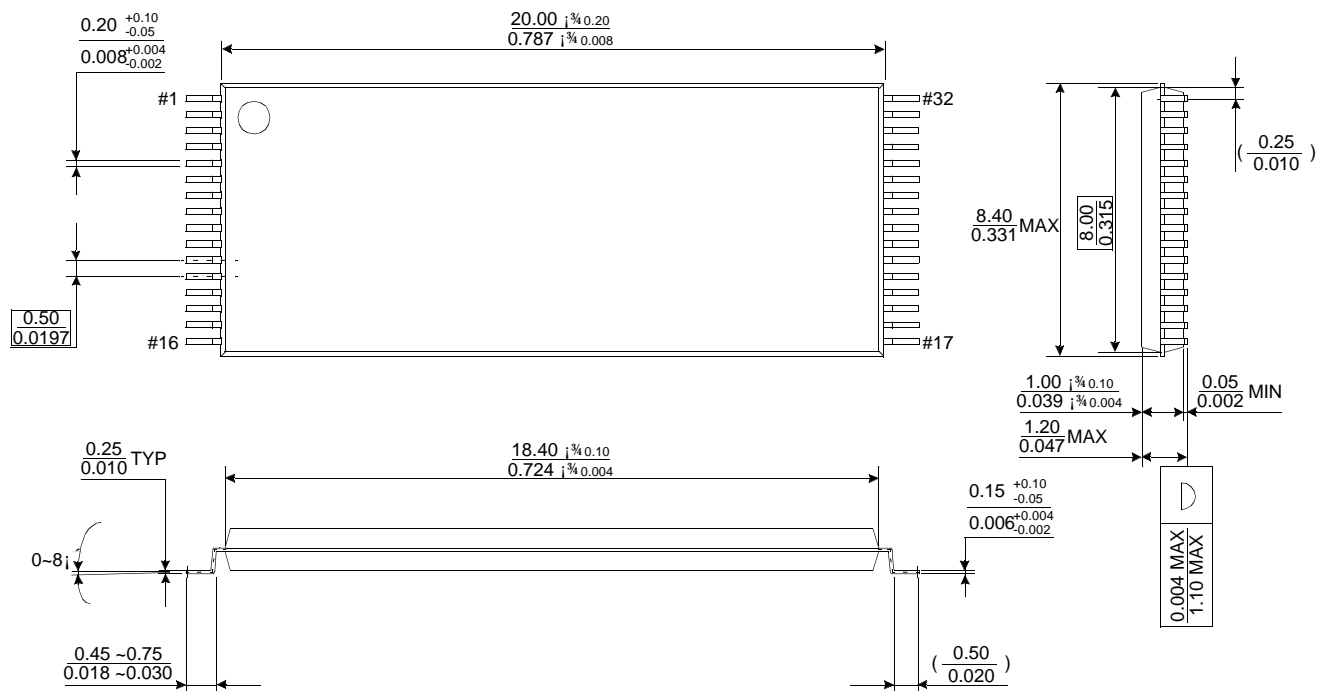
32 DUAL INLINE PACKAGE (600mil)



32 PLASTIC SMALL OUTLINE PACKAGE (525mil)



32 THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



32 THIN SMALL OUTLINE PACKAGE TYPE I (0820R)

